In the Claims:

73) (Currently Amended) A communication interface comprising n data lanes, said interface sequentially transmitting a header distributed across a plurality of said data lanes, a variable amount of payload data distributed across a plurality of said n data lanes;

said header includes transmitting a START symbol on first said data lane, and the transmission of said payload data is followed by an END symbol on at least one said data lane;

said payload data includes transmitting data across said n data lanes up to data lane m, where m<=n;

and said n > 1.

74) (New Claim) The communication interface of claim 73 where said n is 4.

75) (New Claim) A process for transmitting data on a communications channel, said data comprising a header and variable length payload, the channel having a first, a second, a third, and a fourth data lane, each data lane being 8 bits wide and including a clock for transferring said 8 bits, said process comprising the steps:

a first step of sending a synchronization symbol on all four said data lanes for a synchronization interval, or until said variable length payload is ready to be transmitted;

a second step of substantially simultaneously sending said header to said first data lane and part of said payload to the remaining three said data lanes;

a third step of incrementally transmitting the remainder of said payload data in a sequence of transmission events, each said transmission event comprising substantially simultaneously sending said incremental payload data in said four data lanes until final data comprising zero data, one data lane, two data lanes, or three data lanes of said payload data remains to be transmitted;

a fourth step of transmitting said final data accompanied by an END symbol on one said data lane.

76) The process of claim 75 where said final data comprises zero said data lanes and said END symbol is transmitted on said first data lane.

77) The process of claim 75 where said final data comprises zero said data lanes and said END symbol is transmitted on said first data lane accompanied by said

preamble transmitted on said second, said third, and said fourth data lanes.

78) The process of claim 75 where said final data comprises first said data lane and said END symbol is transmitted on said second data lane.

79) The process of claim 75 where said final data comprises first said data lane and said END symbol is transmitted on said second data lane accompanied by said preamble transmitted on said third and said fourth data lanes.

80) The process of claim 75 where said final data comprises said first and said second data lanes and said END symbol is transmitted on said third data lane.

81) The process of claim 75 where said final data comprises said first and said second data lanes and said END symbol is transmitted on said third data lane accompanied by said preamble transmitted on said fourth data lane.

82) The process of claim 75 where said final data comprises first, second, and third said data lanes and said END symbol is transmitted on fourth said data lane.

83) The process of claim 75 where said final data comprises said first, said second, and said third data lanes and said END symbol is transmitted on said fourth data lane accompanied by said preamble transmitted on said fourth data lane.

84) The process of claim 75 where each said clock rate is substantially 312.5Mhz.

85) The process of claim 75 where each said clock rate is 156.25Mhz and both a both positive edge and a negative edge are used to transfer said data.

86) The process of claim 75 where each said clock rate is 312.5Mhz and either a positive edge or a negative edge is used to transfer said data.

87) The process of claim 75 where each said data lane is encoded and serialized into a serial stream of data.

88) THe process of claim 87 where said encoder is an 8B/10B encoder.

89) The process of claim 87 where said serial stream of data is transmitted as a differential electrical signal.

90) The process of claim 87 where said serial stream of data is transmitted as an optical signal.

91) A transmitter for sending data comprising a header followed by a variable length payload, said data being substantially simultaneously transmitted on a first data lane, a second data lane, a third data lane, and a fourth data lane in a succession of time sequences, wherein said variable length data is incrementally transmitted on said first, said second, said third, and said fourth data lanes during each said time sequence in the following manner:

sending a preamble on said first, said second, said third, and said fourth data lanes until said variable length data is ready to transmit, and when said data is ready to transmit:

sending a START symbol on said first data lane and said variable length data on said second, said third, and said fourth data lanes during one said time sequence;

sending the remainder of said variable length payload on said first, said second, said third, and said fourth data lanes during successive said time sequences until there is

insufficient data to send on all four said data lanes, said insufficient data being final data;

when there is no said final data to send, sending said END symbol on said first lane, and said preamble on said second, said third, and said fourth lanes;

when said final data comprises one said data lane, sending said final data on said first lane, an END symbol on said second lane, and said preamble on said third and said fourth lanes;

when said final data comprises two said data lanes, sending said final data on said first and said second lane, an END symbol on said third lane, and said preamble on said fourth lane,

when said final data comprises three said data lanes, sending said final data on said first, said second, and said third lane, an end symbol on said fourth lane.

92) The transmitter of claim 91 where each said data lane is 8 bits wide.

93) The transmitter of claim 91 where each said data lane is 8 bits wide and is clocked at a rate of 312.5Mhz.

94) The transmitter of claim 93 where said 312.5Mhz clock comprises both the positive edge and the negative edge of a 156.25Mhz clock.

95) The transmitter of claim 93 where said 312.5Mhz clock comprises a positive edge or a negative edge of said 312.5Mhz clock.

96) The transmitter of claim 93 where each said data lane includes an encoder and a serializer, each said data lane generating a serialized stream of data.

97) The transmitter of claim 96 where each said data lane includes an encoder receiving data at said time sequence of substantially 312.5Mhz, and each said serializer is clocked at a rate of 10 times said encoder time sequence rate.

98) The transmitter of claim 96 where each said encoder uses 8B/10B encoding.

99) The transmitter of claim 93 where each said data lane comprises 8 bits of data and one bit of clock, said clock operating at a rate of substantially 312.5Mhz.

100) The transmitter of claim 93 where data from each said data lane is transmitted least significant bit first and most significant bit last.

101) The transmitter of claim 93 where data from each said data lane is transmitted most significant bit first and least significant bit last.

102) A transmitter for generating four streams of serial data, said transmitter including:

a transmit buffer for receiving 32 bits of data and separating said 32 bits of data into four data lanes, each comprising 8 bits of data and a clock operating at substantially 312.5Mhz;

each data lane having:

an encoder for converting said 8 bits of data accompanied by said clock into 10 bits of encoded data;

a serializer for transmitting said 10 bits of encoded data into a stream of serial data clocked at 10 times said encoder clock rate.

103) A receiver for converting four streams of serial data into a series of 32 bit words, each said serial stream operating at substantially 3.125 Ghz, said receiver having:

four input data processors, each said data processor having:

a deserializer for converting a stream of serial data into said 10 bits of parallel encoded data and a clock at substantially 312.5Mhz;

a decoder for converting said 10 bits of parallel encoded data into 8 bits of decoded data;

a transmit buffer coupled to each said decoder and each said clock, said transmit buffer converting said 8 bits of decoded data from each said decoder and each said clock into a succession of said 32 bit words.

104) A receiver for converting four streams of serial data and converting said four streams of serial data into a variable length data payload, said receiver comprising:

four deserializers, each said deserializer coupled to a respective serial stream, each said deserializer converting said stream of serial data into 10 bits of encoded data accompanied by a clock for each said serial stream;

four decoders, each said decoder coupled to a respective said deserializer output, each said decoder converting each said 10 bits of encoded data into 8 bits of decoded data, thereby producing 8 bits of decoded data accompanied by a clock;

an elasticity buffer coupled to each said 8 bit decoder data and decoder clock, said elasticity buffer receiving 32 bits of data at a rate of substantially 312.5Mhz, and combining said 32 bits of data over successive intervals to produce said variable length packet.

105) The receiver of claim 104 where said decoder is an 8B/10B decoder.

106) The receiver of claim 104 where said variable length payload is formed using data received on the other three said decoders following a START symbol on one said decoder, thereafter using data from all four said decoders until receipt of an END symbol on any said decoder.

107) The receiver of claim 104 where said variable length payload is formed using data between a START symbol on one said decoder and an END symbol received on any said decoder.

108) The receiver of claim 104 where said elasticity buffer forms said variable length payload by concatenating data received from a first decoder, a second decoder, a third decoder, and a fourth decoder, where a START symbol is received on a first decoder and said variable length packet

is formed from concatenating said data in sequence from said second decoder, said third decoder, said fourth decoder, and said first decoder, repeating until terminated by the receipt of an END symbol on any decoder.

109) The receiver of claim 104 where each said serial stream of data is derived from a differential electrical signal.

110) The receiver of claim 104 where each said serial stream of data is derived from an optical signal.

111) The receiver of claim 104 where said 312.5Mhz clock is the result of using both the rising edge and falling edge of a 156.25Mhz clock.

112) A process for generating a variable length packet from four streams of serial data, the process comprising:

deserializing each said serial stream into 10 bit encoded data, thereafter converting said 10 bit encoded data into four data lanes of 8 bit data, and forming a variable length packet as follows:

a first step of receiving a START symbol on said first data lane and said ordered variable length data on said

second, said third, and said fourth data lanes during one said time sequence;

a second step of receiving the remainder of said variable length payload on said first, said second, said third, and said fourth data lanes during successive said time sequences until an END symbol is detected on one of said data lanes;

thereby forming a variable length packet from said data from said START symbol to said END symbol, also maintaining the order of said data received on said first, said second, said third, and said fourth data lanes.

113) The process of claim 112 where each said decoder is a 10B/8B decoder.

114) The process of claim 112 where each said 8 bit wide data lane is clocked at substantially 312.5Mhz.

115) The process of claim 112 where each said data lane is clocked at substantially 1/10th the rate of each said serial data.

116) The process of claim 114 where said 312.5Mhz clock comprises using either the rising edge or the falling edge of a 312.5Mhz clock.

117) The process of claim 114 where said 312.5Mhz clock comprises using both the rising and falling edge of a 156.25Mhz clock.

118) The process of claim 112 where each said serial stream of data is derived from a differential electrical signal.

119) The process of claim 112 where each said serial stream of data is derived from an optical signal.